

## 3D IC INTEGRATION AND PACKAGING%0A

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bridge to full 3D IC integration in some applications, but they will remain a viable enabling technology for new applications requiring high-density 3D package integration architectures.

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[New 3D Packaging and Integration Committee | SEMI.ORG](#)

New 3D Packaging & Integration Committee. By James Amano, International Standards, SEMI The SEMI International Standards Committee, at their SEMICON West 2017 meeting, approved the transformation of the existing 3D Stacked IC Committee and Assembly & Packaging Committee into a single, unified 3D Packaging

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and Integration Committee.

3D IC Packaging3D IC Packaging and 3D IC Integration - IEEE

For device wafers of 3D IC integration applications, the TSVs are better fabricated by the via-middle process, i.e., after the FEOL to make the devices and MOL to Three-dimensional integrated circuit - Wikipedia Types 3D ICs vs. 3D packaging. 3D Packaging refers to 3D integration schemes that rely on traditional methods of interconnect such as wire bonding and flip chip to achieve vertical stacks. 3D packaging can be disseminated further into 3D system in package (3D SiP) and 3D wafer level package (3D WLP).

3D IC High Performance Packaging & Integration

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